MASENO UNIVERSITY

UNIVERSITY EXAMINATIONS 2016/2017

FOURTH YEAR FIRST SEMESTER EXAMINATION FOR DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE TECHNOLOGY

MAIN CAMPUS

SCS 410: MICROPROCESSOR SYSTEMS

Date: 30th November, 2016 Time: 12.00 - 3.00pm

INSTRUCTIONS:

- Answer Question ONE and any other TWO.

QUESTION ONE (30 MARKS)

a) The Intel 8086 is a 16-bit processor, with a 20-bit address bus. The 8085, the immediate predecessor of the 8086, is an 8-bit processor with a 16-bit address bus. The 8085 operates at 3 MHz with a CPI of 8, while 8086 operates at 8 MHz and a CPI of 5. Compare the performance of these two processor on the basis of
   i. Data and address bus widths
   ii. MIPS rating **[8 marks]**

b) With the aid of a block diagram sketch, describe the register programming model of the 8086 processor. **[5 marks]**

c) Draw the instruction state diagram for a typical microprocessor, and explain how handling an instruction such as *MOV AX, [245D]* can be incorporated. Indicate also and explain how interrupts alter this cycle. **[6 mks]**

d) With reference to pin outs of 8086, explain the differences between Minimum and Maximum modes of operation. **[6 mks]**

e) Describe the stack operation of the 8086. **[2 mks]**
   Given SP = 1236H, AX = 35A8H, DI =58C5H, and DX =5FA2H, show the contents of the stack as each of the following instructions is executed.
   i. PUSH AX
   ii. PUSH DI
   iii. PUSH DX **[6 mks]**

QUESTION TWO (20 Marks)

a) Draw the block diagram of the Intel 8086 processor and use it to describe the functional and operational details of the processor, with specific regard to the EU an BIU **[6 mks]**

b) Describe the instruction queue of the 8086 processor. Hence describe how the EU and the BIU collaborate in effecting a basic pipelining concept. **[6 mks]**
   If the processor has an instruction cycle comprising Fetch, Decode, Execute and Store and that each stage of the cycle requires 10 clock cycles, determine the total execution times for three instructions.
   i. Without the instruction queue pipelining **[3 marks]**
   ii. With instruction queue pipelining, assuming a clock speed of 5 MHz. **[5 mks]**

QUESTION THREE (20 Marks)

a) With the aid of an illustrated sketch, describe the memory organization of Intel 8086 processor. Show clearly all the relevant pins. **[6 mks]**

b) The 8086 processor is executing the following instruction code sequences. Analyze, in each case, the behavior of the processor in accessing the memory, highlighting any performance issues. Use suitable sketches.

i. MOV BX, [00520] **[2 marks]**

ii. MOV BX, [00521] **[4 marks]**

c) Draw the timing diagram for 8086 READ cycle for the instruction MOV AX, 1234H. Highlight the role of the major pin signals. **[8 mks]**

QUESTION FOUR (20 Marks)

a) Identify the addressing modes in the following Intel 8086 instructions and determine the physical addresses in each case. Show the physical address calculations clearly.

i. *MOV AX, 2550H*, given (DS) = 46BCH

ii. *MOV [SI], AX*, given (DS) = E35CH, (SI) = 2498H, (AX) = 19F1H. Show the contents of the memory location after executing the instruction.

iii. *MOV DX, [SI]+5*, given (DS) = 5781H, (SI) = 4321H. **[8 mks]**

b) Describe, with the aid of an illustration, the instruction format of the Intel 8086 processor. **[6 mks]**

c) Encode the instruction *MOV DL, CL*, given that opcode is *100010* **[6 mks]**

QUESTION FIVE (20 Marks)

a) Outline the 8086 input/output techniques and hence compare the merits and demerits of these techniques. **[6 marks]**

b) Explain, with the aid of assembly code segments, the differences between Isolated Input/output and memory mapped input/output mechanisms in 8086 processor. **[4 mks]**

c) Explain the utility and function of the READY and WAIT pins of the 8086 in interfacing with peripherals. **[5 marks]**

d) Consider the timing diagrams shown in *figures a* and *b* below. *Figure a* is the 8086 READY input timing and *figure b* is the 8284A RDY input timing. Comment on the relationship between the two timing diagrams, and justify the values shown. **[5 marks]**

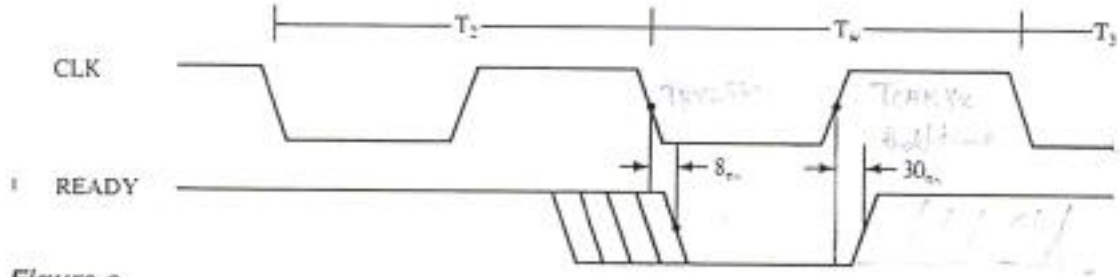

Figure a

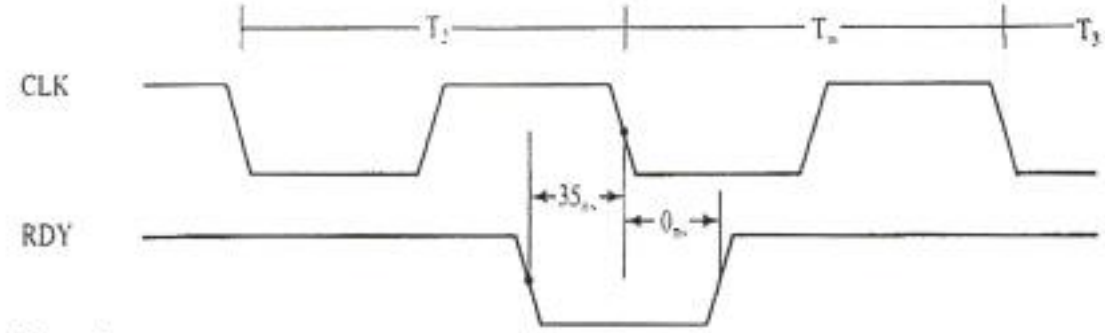

Figure b