# MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY

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**University Examinations 2014/2015**

SECOND YEAR, FIRST SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER TECHNOLOGY.

**BCT 2206: DIGITAL ELECTRONICS**

**DATE: DECEMBER 2014** **TIME: 2 HOURS**

**INSTRUCTIONS:** *Answer question **one** and any other **two** questions*

## QUESTION ONE (30 MARKS)

a) Convert $(2F9A)_{16}$ to its equivalent binary numbers (2 marks)

b) What are k-maps? (2 marks)

c) Prove that $A\overline{B} + \overline{A}B + A = A + B$ (3 marks)

d) State three applications of flip-flops (3 marks)

e) Draw the logic circuit of a full-adder and hence prepare its truth table. (5 marks)

f) Design a logic circuit to realize this function Y= $\overline{\left(\overline{A}B + \overline{B}\overline{C}\right)}$ (3 marks)

g) Implement a NOT gate using NOR gates only (3 marks)

h) Differentiate between synchronous and asynchronous logic circuit (4 marks)

i) Define the following terms

(i) Binary counters (2 marks)

(ii) Multiplexers (2 marks)

## QUESTION TWO (20 MARKS)

a) Convert the following logic expressions to a Standard Sum of Products (SOP) form

(i) $\overline{A} + AB + AB\overline{C}$ (3 marks)

(ii) $A\overline{B} + C + \overline{B}C\overline{D} + AC\overline{D}$ (4 marks)

b) Given the logic expression F= $\overline{A}B + \overline{A}\overline{B}\overline{C} + AB\overline{C} + A\overline{B}\overline{C}$

(i) Convert it to a standard sop form (1 mark)

(ii) Map the standard sop expression onto k-map (2 marks)

(iii) Simplify the expression using k-map (3 marks)

c) Develop a truth table for the logic expression Y= $A\overline{B}C + \overline{A}B\overline{C} + ABC$ (3 marks)

d) Find Two's compliment

(i) 1101010 (1 mark)

(ii) 111011010 (1 mark)

e) Add the hexadecimal number 07F+05B (2marks)

**QUESTION THREE (20 MARKS)**

a) Why is S=R=1 not permitted in S-R flip-flops? (2 marks)

b) Design a 3- input shift register and explain how the Binary 110 can be loaded into the registers (6 marks)

c) Explain with help of a truth table the working of a J-K flip-flop (5 marks)

d) (i) Write a count sequence of a 3-bit down counter (2 marks)

(ii) Design a logic circuit of the above sequence (3 marks)

e) State two application of shit registers (2 marks)

**QUESTION FOUR (20 MARKS)**

a) Explain briefly the working of half Adder (4 marks)

b) With the help of a block diagram, explain how the two signals 1.01 and 110 can be added using parallel full Adders (5 marks)

c) Differentiate between a multiplexer and a demultiplexers (4 marks)

d) Design a 64x1 mulitplexer using 16x1 multiplexers

e) State two applications of multiplexers (2 marks)