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University Examinations 2013/2014

SECOND YEAR, SECOND SEMESTER EXAMINATION FOR DIPLOMA IN ELECTRICAL
ENGINEERING

EEE 0233: DIGITAL ELECTRONICS II

DATE: APRIL 2014

TIME: 1 ½ HOURS

INSTRUCTIONS: Answer question *one* and any other *two* questions

QUESTION ONE – (30 MARKS)

- (a) Define the following terms as used in digital electronics
- (i) Flip-flip
 - (ii) Register
 - (iii) Counter (6 Marks)
- (b) Explain clearly the difference between the following
- (i) Combinational and sequential circuits
 - (ii) Racing and toggling (4 Marks)
- (c) Simplify the following expression and show the minimum gate implementation
 $Y = ABC\bar{D} + \bar{A}B\bar{C}D + A\bar{B}C$ (4 Marks)
- (d) With the aid of a logic diagram, explain the operation of the NAND gate latch. (5 Marks)

(e)

The figure above show a transistor logic circuit.

- (i) Describe its operation
 - (ii) Draw its diode equivalent circuit
 - (iii) Draw the truth table for the TTL circuit above. (7 Marks)
- (f) The figure below shows a combinational logic circuit. Derive the Boolean expression for the circuit at point Y. (4 Marks)

QUESTION TWO – (15 MARKS)

- (a) State the Demorgan's theorems. (2 Marks)
(b) Simplify the following expression using Demorgan's theorem

$$\overline{\overline{A(B + \bar{C})}D} \quad (3 \text{ Marks})$$

- (c) Discuss NOR gate as a universal gate. Hence or otherwise draw the truth table and electronic switching circuit of NOR gate. (10 Marks)

QUESTION THREE – (15 MARKS)

- (a) Simplify the following Boolean expression using the Karnaugh Mapping technique
 $X = \bar{A}B + \bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$ (5 Marks)
(b) Draw and explain the working a master-slave J-K flip flop using NINE NAND gates.
Explain how the race around problem is eliminated in the master-slave J-K flip flop. (10 Marks)

QUESTION FOUR – (15 MARKS)

- (a) Discuss the two types of registers. (8 Marks)
(b) Draw and explain the working of a 4-bit binary ripple counter. (7 Marks)