2207/304
DIGITAL PRINCIPLES AND MICROPROCESSORS
Oct./Nov. 2010
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS
(COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
Electronic calculator;
Intel 8085 instruction set.

Answer any FIVE of the EIGHT questions in this paper.
All questions carry equal marks.
Maximum marks for each part of a question are as shown.

This paper consists of 6 printed pages.

**Candidates should check the question paper to ascertain that
all the pages are printed as indicated and that no questions are missing.**

1. (a) (i) Perform the following multiplication in the given base without converting first into decimal; show all the working.

$$(32)_4$$
$$\times \ (23)_4$$

(ii) Perform the following arithmetic operations in the given bases:

I. $(73462)_8$
$-(57647)_8$

II. $6EF2_{16}$
$+3EDF_{16}$

(7 marks)

(b) Represent the decimal number 8730 in;

(i) BCD;
(ii) excess - 3 code;
(iii) 2,4,2,1 code;
(iv) binary.

(9 marks)

(c) Represent the decimal number -157 in binary:
(i) Sign-magnitude form;
(ii) TWO's complement.

(4 marks)

2. (a) Use the boolean algebra postulates and theorems to minimise the following expressions.

(i) $XYZ + \bar{X} Y\bar{Z} + \bar{X}YZ + XY\bar{Z} + \bar{X} Y \bar{Z}$;
(ii) $AB + CB + CAB + ABD$;
(iii) $(\overline{\overline{CD}} + A) + A + CD + AB$.

(9 marks)

(b) For the following boolean function:

$$f(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 9, 12, 14)$$

(i) draw the truth table;
(ii) draw a K-map representation of the function;
(iii) simplify and state the output function as a sum of products. (11 marks)

3. (a) (i) Draw a circuit diagram of a CMOS NAND gate and describe its operation.
(ii) State any **two** advantages of CMOS gates. (8 marks)

(b) A logic circuit is required to convert a BCD decimal number to its excess - 3 equivalent.

(i) draw a truth table for BCD to excess - 3 code;

(ii) explain, using a labelled schematic block diagram, how an adder circuit can be be used to achieve the conversion in b(i). (12 marks)

4. (a) (i) Distinguish between synchronous and asynchronous counters.
(ii) A 10MHZ clock is applied to a cascaded asynchronous counter consisting of a modulo 5 counter followed by modulo 8 counter.
Determine the:

I. modulo of the cascaded counter;

II. frequency of the waveform at the output of the most significant flip-flop. (7 marks)

(b) You are to implement a 3 - bit gray code counter using JK - flip-flops.
(i) draw the excitation table of the JK - flip-flop;
(ii) draw a state table of the counting sequence and the corresponding JK inputs.
(iii) derive minimised flip-flop input functions for the counter;
(iv) draw a logic circuit diagram of the gray code counter. (13 marks)

5. (a) Describe the following as applied to microcomputer memory:
(i) memory map;
(ii) dynamic. (4 marks)

(b) With the aid of a schematic block diagram, show how 1K X 8 RAM IC's can be connected to provide 4k x 8 RAM memory. (8 marks)

(c) (i) For a DRAM memory, describe the functions of any control signals.

(ii) State any **two** advantages of DRAM memory. (8 marks)

6. (a) A digital to analogue converter (DAC) has a resolution of 0.01% and operates with + 20V reference voltage. Determine the:

  (i) number of input binary bits;
  (ii) input binary bits pattern for the half scale analogue output voltage.

(5 marks)

  (b) Define the following with respect to interrupts;

  (i) masked;
  (ii) edge-triggered;
  (iii) vector address.

(3 marks)

  (c) (i) Differentiate between memory-mapped and I/O mapped input-outputs.

  (ii) Describe each of the following microprocesssor signals:

  I. Hold;
  II. $\overline{READY}$;
  III. ALE;
  IV IO/$\overline{M}$.

(12 marks)

7. (a) For each of the following 8085 instructions:
  I. STA 2000H;
  II. MOV A, M;
  III. MVI H, 30H;
  IV. MOV B, A

  (i) identify the addressing mode;
  (ii) state the size, in bytes, of the machine code instruction.

(8 marks)

  (b) The programme shown in Table 1 is a listing of instruction in hexadecimal code.
  The computer executes the instructions starting from location 2000H.
  (i) di-assemble the program into symbolic form;
  (ii) determine the contents of register A at the end of program execution;
  (iii) explain what the program accomplishes.

(12 marks)

Table 1

Location (Hex)	Instruction (Hex)
2000	3E
2001	02
2002	87
2003	47
2004	87
2005	87
2006	80
2007	76

8. (a) (i) Describe the checksum method of testing microcomputer ROM memories.
    (ii) Explain the drawback of the method in a(i).

(6 marks)

(b) (i) Draw the truth-table of a 2 - to - 4 decoder.
    (ii) Describe how to test the correct operation of the decoder in b(i) using a multimeter.
    Assume the decoder is TTL.

(6 marks)

(c) With the aid of block diagram and waveforms, describe how a signature analyser is used in diagonising faults in microprocessor based systems.

(8 marks)

Instruction set of 8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LXI B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	..
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SP,D16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	..	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	---	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	90	SUB B	BB	CMP E	E6	ANI D8
10	---	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	---
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	XRI D8
18	---	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DCR E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	---	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	..
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	..	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.